CERTIFICATE OF TRANSMISSION BY FACSIMILE (37CFR1.8)

PLEASE DELIVER TO TIMOTHY COLE, PATENT APPEAL CENTER SPECIALIST

Docket No. END920010118US2 (IEN-10-5625-D1)

Applicant(s): Day et al

Serial No.	Filing Date	Examiner	Group Art Unit
10/616,341	July 9, 2003	Jayme L. Brown	1733

Invention:

SELECTIVELY ROUGHENING CONDUCTORS FOR HIGH FREQUENCY PRINTED WIRING BOARDS

I hereby certify that this **Response to Notification of Non-Compliant Appeal Brief** and **AMENDED APPEAL BRIEF** are being transmitted via facsimile to the United States Patent and Trademark Office.

Fax. No. 571-273-8300 on OCTOBER 26, 2006 *(Date)* 17 *(No. of pages)*

TO: Timothy Cole
Patent Appeal Center Specialist

Attached is an Amended Appeal Brief being filed in response to your Notification of Non-Compliant Appeal Brief issued October 4, 2006.

It is not believed that any fees are required. However, the Commissioner is hereby authorized to charge payment of fees associated with this communication, or credit any overpayment. to Deposit Account No. 500645.

FROM: William N. Hogg
CUSTOMER NO. 26681

Carole *Giacomazzo*

(Typed or Printed Name of Person Signing Certificate)

(Signature)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of Day et al		:	
Serial No.	10/616,341	:	Art Unit 1733
Filed:	July 9, 2003	:	Examiner J. H. Aftergut
Title:	**SELECTIVELY ROUGHENING CONDUCTORS FOR HIGH FREQUENCY PRINTED WIRING BOARDS**	:	Confirmation No. 1504

Atty. Docket No. END920010118US2 (IEN-10-5625-D1)

RESPONSE TO NOTIFICATION OF NON-COMPLIANT APPEAL BRIEF

(37 CFR 41.37)

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Attention: Timothy Cole, Patent Appeal Center Specialist

Dear Sir:

Responsive to the Patent Office Notification of Non-Compliant Appeal Brief, Applicants are submitting the attached Amended Appeal Brief which complies with the requirements listed in items 2, 4 and 10. It is believed that the Appeal Brief is now in proper form for entry and consideration.

It is not thought that any additional fees are due, the appeal fee having already been paid. However, the Commissioner is authorized to charge Deposit Account 500645 should fees be due.

Respectfully submitted,

Date: OCTOBER 11, 2006

William N. Hogg, Reg. No. 20,156
CUSTOMER NO. 26681WNH:cg

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of Day et al		:	
Serial No.	10/616,341	:	Art Unit 1733
Filed:	July 9, 2003	:	Examiner J. Aftergut
Title:	**SELECTIVELY ROUGHENING CONDUCTORS FOR HIGH FREQUENCY PRINTED WIRING BOARDS**	:	Confirmation No. 1504

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AMENDED APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-entitled application is International Business Machines Corporation of Armonk, New York.

II. RELATED APPEALS AND INTERFERENCES

The undersigned attorney is not aware of and, on information and belief, neither the appellants nor the assignee is aware of, any related appeals or interferences which would directly affect, or be directly affected by, or have a bearing on the Board's decision in this pending appeal.

III. STATUS OF THE CLAIM(S)

Claims 1 and 3-15, all of the claims in the application, have been finally rejected and are all appealed. Claim 2 has been canceled. No claims have been allowed.

IV. STATUS OF AMENDMENTS

All proposed amendments have been entered, so no issues as to entry of amendments are present.

V. SUMMARY OF THE INVENTION

It has been found that roughening of the conductors on the printed wiring board structure is critical only in certain regions and not required for the entire length of each of the circuit traces or signal lines. In fact, the mechanical and chemical exposures are greatest where a signal or power plane intersect a plated through hole. Therefore, the need is greater for good copper to laminate adhesion at this intersection than in the open, non-drilled areas of the board. (Unless otherwise noted, Figures 1-3 depict the invention as claimed--) (Page 2, line 10 - page 3, line 8). Thus, according to the present invention, a printed wiring board is formed from two or more layers **10, 12** of dielectric material by sticker sheet **13**, one of which layers **10** has circuit lines or traces **14** formed thereon, and wherein the surfaces of the circuit lines or traces are selectively roughened, i.e. the lands **16**, as shown at **25** only in those areas that require very good copper to laminate adhesion, whereas the remainder of the surface of the circuit lines or traces **14** is maintained in essentially a smooth condition **18.** "Smooth" generally refers to an R_z measurement of less than about 1 micron. The term "rough" as used herein generally refers to a surface that has an R_z measurement of greater than about 3 microns. Mean roughness depth R_z is the arithmetic mean value of the single roughness depths R_z (i), where R_z(i) is the vertical

distance between the highest peak and the deepest valley within consecutive sampling lengths. The terms "R_z" or "R_z(DIN)" are set forth in ASME B46.1-1995 or ISO 4287-1997.) This provides a good solution to the conflicting needs for good adhesion and good signal propagation qualities since there is only a limited or relatively small area that requires very good adhesion, and these areas are generally so small that they do not materially affect the propagation of the signals on the signal lines (page 3, line 1-7). Thus, those critical areas for propagation of the signal on signal lines or traces can have the circuit lines or traces smooth to maximize the signal propagation effect, while those limited areas where the signal propagation is not critical can be roughened so as to improve the adhesion of one layer to another. Therefore, in the resulting board, adequate adhesion can be obtained while still providing a significantly better signal propagation than is possible with the roughened conductor surface (page 2, line 15 - page 3, line 7).

It has also been found that on the voltage planes **26** (including power and ground planes) smoothing the surface of the voltage plane in those regions opposite the smooth surface regions of the signal planes improves the performance of the signal propagation. The voltage plane 26 in the normally manufactured condition has a roughness of less than an R_z value of 1 micron on the surface facing away from the dielectric material 27. . In this technique, the voltage plane 26 is covered with a photoresist 44 after the opening 29 has been formed. Again, the photoresist is selectively exposed and the areas that are to be roughened are developed to expose the portion 36 of the voltage plane 26 through openings 46, as shown in Figure 8. (page 7, lines 5-11). Thus, these limited areas of the voltage planes can be maintained smooth while the other areas of the surface of the voltage planes can be roughened, which provides the necessary adhesion of the

voltage plane to the adjoining layer of dielectric material between the voltage plane and the signal plane (page 7, line 12-13).

In the case of both signal and voltage planes, the application of selective roughening is not necessarily dictated solely by the location of signal lines and plated through holes, but can be customized for a specific board design by balancing the electrical signal performance characteristics and mechanical requirements of that board. For example, one design may require smooth conductors on every signal line and the respective area of the reference planes, another design may prescribe smooth conductors on the signal lines only and not the reference planes, while still another may have only a few select number of signal lines requiring smooth conductors for optimum electrical performance, allowing all other conductors roughened for maximum mechanical adhesion (page 3, line 15 - page 4, line 2).

Sticker sheet **13** is disposed between the signal layer **10** and the reference voltage layer **12** to which the signal layer **10** and reference voltage layer **12** are laminated by conventional means. The sticker sheet **13** is maintained in the B cured state (partially cured) for lamination, after which the laminate is fully cured. During drilling of holes at the composite level, opening **32** is formed through sticker **13** aligning with opening **17** in dielectric **15** and opening **28** in dielectric **27** so that a continuous through opening is provided. The openings **32, 29** and **17** provide the surface for plated through hole 33 which comprises copper plated onto the dielectric materials in a conventional manner. The land **16** is in contact with the copper **33** in the openings **17, 29** and **32** to provide for a signal path. The copper plating **33** includes annular collars on opposite sides of the laminate structure.page 7 line 18 - page 8 line 6) (It is to be understood that the printed wiring board shown in Figures 1-3 is for illustrative purposes only and that

several different layers could be, and typically are, stacked but the showing only of the layers **10** and **12** illustrates the present invention.)(page 8 lines 6-9)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The examiner has rejected claims 1 and 3-15 (all of the claims pending in the application) as being unpatentable under 35 U.S.C. 103(a) over appellants' admitted prior art, hereinafter AAPA, in view of Japanese Patent 2000-68620, hereinafter 620, and Gerber et al, U.S. Patent 5,401,913, hereinafter Gerber et al. This rejection is not thought to be well taken.

VII. ARGUMENTS

Claim 1

First, claim 1, upon which all of the other claims depend, directly or indirectly, requires a voltage plane as a sheet of foil disposed on a dielectric, and laminating the voltage plane to the signal plane with a sticker sheet therebetween. It is respectfully submitted that although the AAPA does disclose a circuit board wherein the signal traces are generally roughened, none of the prior art suggests the structure shown by the AAPA, Gerber et al, or 620, or any reasonable combination thereof. With respect to Gerber et al, no voltage plane is shown in relationship to the signal lines, and the films of material **58, 24, 60** and **62** may be an anisotropically *conductive* adhesive (Column 6, lines 36-39). This is not a sticker sheet or a voltage plane.

A sticker sheet is a dielectric material, page 7, lines 20-22. Since there is no voltage plane shown in the prior art, it cannot be oriented toward the signal plane. Thus, the references do not show or teach the invention as claimed.

Moreover, at the locations cited by the examiner of the 620 patent, namely paragraphs [0011], [0012] and [0065], it appears that the roughening of the lands is to obtain better connection of the lands to other conductive material.

> "[0011] According to the 1st above-mentioned configuration, since the contact interface with the conductive constituent of a circuit pattern is roughened, a touch area increases and the dependability of connection improves according to the operation which the number of points of contact of the conductive filler in a conductive constituent and the metallic foil of a circuit pattern increases, or heightens adhesive strength of the resin and the circuit pattern which are contained in a conductive constituent."

Since the translation furnished by the Patent Office was done by a machine, it is difficult to understand it completely. However, the English language version of the Abstract states as follows:

> "PROBLEM TO BE SOLVED: To realize a circuit substrate having high reliability in inner via hole connection by a method wherein at least one of interfaces of a wiring pattern with a conductive component is roughened more than an interface with an insulator layer." (Emphasis supplied)

Thus, it is clear that in appellants' case, the roughening of the conductor is for adhesion to a *dielectric material*, i.e. the substrate or sticker sheet, not a *conductive material* as in the 620 patent. This function is clearly shown in the drawings, especially in Figures 1 and 2, and set out on page 2, lines 15-19 of the instant case:

> "Thus, according to the present invention, a printed wiring board is formed from two or more layers, one of which has circuit lines formed thereon, and wherein the surfaces of the circuit lines or traces are selectively roughened only in those areas that require very good copper to laminate adhesion, whereas the remainder of the surface of the circuit lines or traces are maintained in essentially a smooth condition."
> (Emphasis supplied)

The reasons for smooth and roughened surfaces are explained in detail on page 1, line 13, through page 2, line 13, of the instant application. None of these reasons apply to the art cited by the examiner and, thus, there cannot be any motivation to combine the references for roughening a surface for adhesion to a dielectric material.

It is not enough that one may modify a reference in view of a second reference, but rather it is required that the second reference suggest modification of the first reference and not merely provide the capability of modifying the first reference.

The CAFC stated in In re Piasecki, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984) the following:

> "The Supreme Court in Graham v. John Deere Co., 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure, Graham is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103'. Citing In re Warner, 379 F.2d 1011, 1020, 154 USPQ 173, 177 (CCPA 1967)."

The law is quite clear that in order for a claimed invention to be rejected on obviousness, the prior art must suggest the modifications sought to be patented; In re Gordon, 221 U.S.P.Q. 1125, 1127 (CAFC 1984); ACS Hospital System, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (CAFC 1984). The foregoing principle of law has been followed in Aqua-Aerobic Systems, Inc. v. Richards of Rockford, Inc., 1 U.S.P.Q. 2d, 1945 (D.C. Illinois 1986). In the Aqua-Aerobic's case, the Court stated that the fact that a prior reference can be modified to show the claimed invention does not make the modification obvious unless the prior reference suggests the desirability of the modification. The CAFC in the case of In re Gorman, 18 U.S.P.Q. 2d (CAFC 1991) held at page 1888:

> "When it is necessary to select elements of various teachings in order to form the claimed invention, we ascertain whether there is any suggestion or motivation in the prior art to make the selection made by the applicant [citation]. 'Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion, or incentive supporting the combination' [citations]. . ..
>
> The references themselves must provide some teaching whereby the applicant's combination would have been obvious."

Further, the CAFC, in In re Oetiker, 24 U.S.P.Q. 2nd 1443, 1445 (CAFC 1992) held:

"There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself."

Most significantly, the CAFC in the case of In re Dembiczak, 50 U.S.P.Q.2nd 1614 (CAFC 1999) held at 1617:

"...(examiner can satisfy burden of obviousness in light of combination 'only by showing some objective teaching [leading to the combination]')"

Thus, it is clear that where an individual reference does not teach the entire invention, then the modification which the invention represents must be suggested and motivated by some other reference through some objective teaching and cannot come from the application itself, which is not the case here. The mere suggestion of selective roughening is not sufficient. Especially since it is at a different place for a different purpose.

Claims 3-15

Claims 3-15 are dependent, directly or indirectly, on claim 1 and, for the same reasons, are believed to be allowable.

Claims 3-5

Moreover, with respect to claims 3-5, there is nothing in the prior art to suggest any degree of roughness or smoothness of the signal plane (page 7, lines 4-11), and there is no suggestion anywhere that the appellants' choices are desirable, or even appropriate. Thus, for this additional reason, claims 3-5 are believed to be allowable.

Claims 8, 9 and 13-15

With respect to claims 8, 9 and 13-15, since there is no suggestion of a voltage plane as related to the signal plane, there is definitely no suggestion of areas of roughness and smoothness and certainly not of that claimed in claim 9 (page 8, lines 10-17). Thus, for this additional reason, these claims are believed to be allowable.

SUMMARY

Therefore, in view of the foregoing, it is respectfully requested that the Board reverse the examiner, and allow claims 1 and 3-15.

Respectfully submitted,

Date: OCTOBER 11, 2006

William N. Hogg , Reg. No. 20,156
CUSTOMER NO. 26681

WNH:cg

Attachments

CLAIM APPENDIX

1. (Previously presented) A method of laminating a circuit board comprising the steps of:

providing a first layer having a dielectric material having a conductive signal plane thereon, said signal plane having at least one surface with a first portion having a first roughness;

forming said signal plane into signal lines and lands;

thereafter selectively roughening at least a second portion of said at least one surface including said lands, but less than all of said one surface, to form a second surface having a second roughness greater than said first roughness;

providing a second layer comprised of a voltage plane as a single sheet of foil disposed on a dielectric material; laminating said first layer to said second layer with a sticker sheet therebetween to form a composite structure; said signal plane and said voltage plane being oriented toward each other;

said composite structure being formed with plated through holes surrounded by said lands.

2. (Canceled)

3. (Previously presented) The invention as defined in claim 1 wherein said second roughness of said signal plane has an R_z value greater than about 3 microns.

4. (Previously presented) The invention as defined in claim 1 wherein the first roughness of said at least one surface of said signal plane has an Rz value of less than about 1 micron.

5. (Previously presented) The invention as defined in claim 1 wherein said first roughness of said signal plane has an R_z value less than about 1 micron, and said second roughness of said signal plane has an R_z value greater than about 3 microns.

6. (Previously presented) The invention as defined in claim 1 wherein said signal plane has a plurality of portions of said at least one signal plane surface with said second roughness.

7. (Previously presented) The invention as defined in claim 6 wherein said plurality of portions of said at least one signal plane surface includes at least three surfaces.

8. (Previously presented) The invention as defined in claim 1 wherein said voltage plane has a first portion with at least one surface with a first surface roughness aligned with the first portion of said signal plane, and a second portion having a second surface with a second surface roughness greater than the surface roughness of said first portion of said voltage plane.

9. (Original) The invention as defined in claim 8 wherein said first portion of said at least one surface of said voltage plane has an R_z value surface roughness of less than about 1 micron and said second portion of said second surface of said voltage plane has an R_z value of greater than about 3 microns.

10. (Previously presented) The invention as defined in claim 1 wherein said second portions of said signal plane having a second roughness are copper and are roughened by treating the copper surface with an oxide or an oxide replacement process, or having plated thereon zinc, brass, nickel or chrome.

11. (Previously presented) The invention a defined in claim 1 wherein said surface of said signal plane having said second roughness is created by applying a photoresist material to said signal plane, then exposing and developing said photoresist to reveal the surface to have said second roughness, then treating said surface to have said second roughness to provide the desired surface roughness, then removing the photoresist.

12. (Previously presented) The invention as defined in claim 1 wherein said second portion on said signal plane having said second roughness is created by,

applying a masking material to unmasked areas of said signal plane that are not to have said second roughness,

then roughening those areas to have said second roughness.

13. (Previously presented) The invention as defined in claim 8 wherein said second portion of said signal plane roughened surfaces having said second roughness and said second portion of said voltage plane having said second roughness are roughened by treating the copper surface with an oxide or an oxide replacement process, or having plated thereon zinc, brass, nickel or chrome.

14. (Previously presented) The invention a defined in claim 8 wherein said surface on said voltage plane having said second roughness is created by applying a photoresist material to said voltage plane, then exposing and developing said photoresist to reveal the surface to have said second roughness, then treating said to have said second roughness surface to provide the desired surface roughness, then removing the photoresist.

15. (Previously presented) The invention as defined in claim 1 wherein said second portion on said signal plane having said second roughness is created by,

applying a masking material to unmasked areas of said signal plane that are not to have said second roughness,

then roughening those areas to have said second roughness.

EVIDENCE APPENDIX

No evidence has been entered.

RELATED PROCEEDINGS APPENDIX

No related proceedings are known to appellants' attorney.